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TITLE: MATRIX TYPE IMAGE DISPLAY DEVICE

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ABSTRACT:
PROBLEM TO BE SOLVED: To provide a high resolution and large-sized matrix type display device capable of inputting a high resolution display signal to respective pixels even during a short display signal input time.

SOLUTION: Each display pixel circuit 14 is provided with a D/A converter 22, and a TN liquid crystal capacitor 23 is connected to the output of the D/A converter 22, and the output of a latch is connected to the input. The timing input of the latch 21 is connected to a Y drive circuit 15 through a gate line 11, and the data input of the latch 21 is connected to an X drive circuit 16 through a data bus 12. The other end of the TN capacitor 23 is connected to a common electrode 24. The Y drive circuit 15 selects successively the gate line of respective rows according to a clock 17 inputted from a control circuit 19 to set it in a high voltage level. A digital display signal is inputted to the X drive circuit 16 through a digital input line 18, and to be outputted to the data bus 12 at every row when digital display signals by one row are collected.

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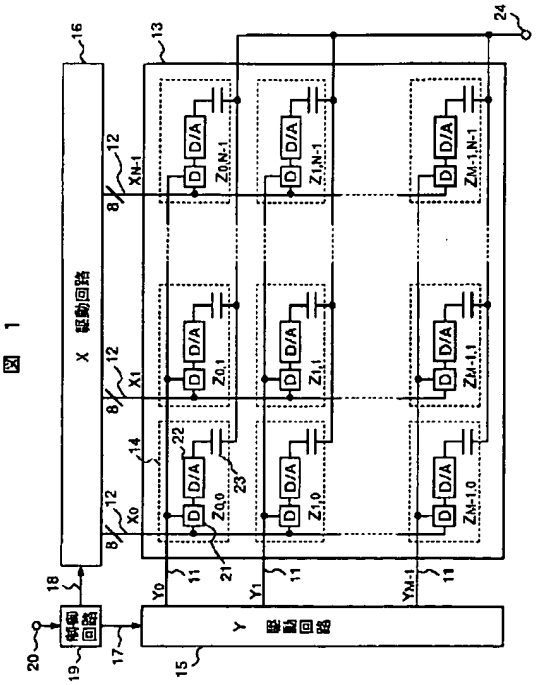
(54)【発明の名称】　マトリクス型画像表示装置

(57)【要約】

【課題】短い表示信号入力時間の間でも各画素に高解像度の表示信号を入力するができ、高解像度の大形マトリクス型表示装置を提供すること。

【解決手段】各表示画素回路１４は、ＤＡ変換器２２を備え、ＤＡ変換器２２の出力にはＴＮ液晶静電容量２３が接続され、入力にはラッチ２１の出力が接続されている。ラッチ２１のタイミング入力はゲート線１１を介してＹ駆動回路１５に接続され、ラッチ２１のデータ入力はデータバス１２を介してＸ駆動回路１６に接続されている。ＴＮ液晶静電容量２３の他端は共通電極２４に接続されている。Ｙ駆動回路１５は、制御回路１９から入力されるクロック１７に従い、順次各行のゲート線１１を選択して高電圧レベルに設定する。Ｘ駆動回路１６にはデジタル表示信号がデジタル入力線１８を経由して入力されており、一行分のデジタル表示信号が揃った時点で、各列毎にデータバス１２に出力される。

図１



1

【特許請求の範囲】

【請求項1】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、前記複数の画像表示素子回路は、各々、DA変換器を有することを特徴とするマトリクス型画像表示装置。

【請求項2】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、前記複数の画像表示素子回路は、各々、マトリクス型画像表示装置の各交点にある画像表示素子回路が、ラッチとDA変換器とを備えていることを特徴とするマトリクス型画像表示装置。

【請求項3】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、前記複数の画像表示素子回路は、各々、CMOSで構成されたDA変換器を備えていることマトリクス型画像表示装置。

【請求項4】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、前記複数の画像表示素子回路には、各々、画像信号がデジタル信号の形式で与えられることを特徴とするマトリクス型画像表示装置。

【請求項5】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、列方向に各画像表示素子回路を接続するデータバスを設け、各画像表示素子回路内にDA変換器を設け、各画像表示素子回路内でアナログデータに変換することを特徴とするマトリクス型画像表示装置。

【請求項6】ガラス基板と、このガラス基板上に、二次元のマトリクス状に配列して形成された複数の画像表示素子回路とからなるマトリクス型画像表示装置であって、列方向に各画像表示素子回路を接続するデータバスを設け、各画像表示素子回路内にDA変換器を設け、さらに、前記DA変換器とデータバスの間にラッチを設けたことを特徴とするマトリクス型画像表示装置。

【請求項7】画素電極と、前記複数の表示画素電極の各々に対応して設けられたラッチ及びDA変換器を含み、前記ラッチのタイミング入力が前記複数の表示画素電極を行単位で走査する信号を供給するゲート線に接続され、前記ラッチのデータ入力が前記複数の表示画素電極に列単位でデジタル表示データを供給するデータバスに接続され、前記ラッチのデータ出力が前記DA変換器の入力に接続され、前記DA変換器の出力が表示画素電極に接続されていることを特徴とするマトリクス型画像表示装置。

【請求項8】二次元のマトリクス状に配列された複数の

2

表示画素電極と、前記複数の表示画素電極の各々に対応して設けられたラッチ及びDA変換器を含み、前記ラッチのタイミング入力が前記複数の表示画素電極を行単位で走査する信号を供給するゲート線に接続され、ラッチのデータ入力が前記複数の表示画素電極に列単位でデジタル表示データを供給するデータバスに接続され、前記ラッチのデータ出力が前記DA変換器の入力に接続され、前記DA変換器の出力が表示画素電極に接続されていることを特徴とするマトリクス型画像表示装置。

【請求項9】前記複数の表示画素電極、前記複数のラッチ、前記複数のDA変換器、前記複数のゲート線、前記複数のデータバスが液晶層を挟持する一対のガラス基板上に形成されていることを特徴とする請求項7に記載のマトリクス型画像表示装置。

【請求項10】前記複数のラッチは、CMOSで構成されたClocked インバータからなることを特徴とする請求項7に記載の画像表示装置。

【請求項11】前記複数のDA変換器は、CMOSで構成された電流切替形からなることを特徴とする請求項7に記載のマトリクス型画像表示装置。

【請求項12】前記複数のラッチ、前記複数のDA変換器は薄膜トランジスタで構成され、液晶層を挟持する一対のガラス基板上に形成されている請求項7に記載のマトリクス型画像表示装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、マトリクス型画像表示装置、特に大型の画面で高解像度表示を可能とするマトリクス型画像表示装置に関する。

【0002】

【従来の技術】従来のマトリクス型画像表示装置として、液晶画像表示装置を例に採り、図10を用いて説明する。図10は、従来の技術による液晶画像表示装置の構成図である。このような従来の画像表示装置の例としては、例えばSID94, Digest of Technical Papers, pp. 359－362, (1994)等が知られている。

【0003】図10において、各々複数本のゲート線111と信号線112との交点にある各画素（画像表示素子）には、透過光量を変調するためのTN（Twisted Nematic）液晶層が設けられているが、これを静電容量105で示している。各画像表示素子回路及びその駆動回路の構成及び動作は、次の通りである。

【0004】静電容量105にはTFT（Thin Film Transistor）スイッチ102が接続されている。TFTスイッチ102のゲートは、ゲート線111を介してシフトレジスタ114に接続されている。また、TFTスイッチ102のドレインは信号線112、DA変換器116を介してラッチ回路115に接続されている。シフトレジスタ114とラッチ回路11

5は、ともに制御回路１１８に接続され、制御回路１１８には信号入力端子１１９が設けられている。なお、ＴＮ液晶静電容量１０５の他端は共通電極１０７に接続されている。

【０００５】シフトレジスタ１１４は、制御回路１１８から入力されるクロックに従い、ゲート線１１１を順次選択して高電圧レベルに設定する。ラッチ回路１１５には1行分の表示信号が入力されており、この表示信号はＤＡ変換器１１６を介して信号線１１２に入力される。シフトレジスタ１１４によってゲート線１１１を介して選択された行のＴＦＴスイッチ１０２はオン状態になるため、選択された行のＴＮ液晶静電容量１０５には、信号線１１２を介して表示信号が入力される。ＴＮ液晶は印加電圧によってその光学特性が制御されるため、図中には省略している偏光板及びバックライトと組み合わせることにより、表示画素マトリクスには画像情報を表示することができる。

【０００６】画像表示装置において、動画の動きを視覚的に滑らかなものとするためには、一般に、フレーム間の表示間隔を１／６０秒以下にすることが必要である。このためには全表示画素に対して１／６０秒以内に表示信号の入力を行う必要がある。一方、高解像度、大画面ののマトリクス型画像表示装置の代表例である、ＳＸＧＡ型画像表示装置では、画素数が１２８０×１０２４画素で、行数は１０２４である。このため、1行あたりの表示信号入力時間は１／６０÷１０２４＝１６．３μｓ以下しか確保することができない。

【０００７】しかるに、上記従来技術によるマトリクス型画像表示装置では、信号線１１２は寄生抵抗、寄生容量を有するため、ＤＡ変換器１１６の出力インピーダンスをいかに小さくしても出力の安定までに過渡時間が必要である。この過渡時間はＤＡ変換器１１６から離れる程大きくなる。画面が大型化すると、さらにこの過渡時間が大きくなる。

【０００８】一方、一本のゲート線１１１が駆動するＴＦＴスイッチ１０２は、ＳＸＧＡ型（１２８０×１０２４画素）高解像度の画像表示装置では１２８０程度にもなる。カラーのものではこの３倍になる。このため、ゲート線１１１に接続される負荷容量は高解像度の画像表示装置では大きくなる。このため、シフトレジスタ１１４の出力インピーダンスをいかに小さくしても、シフトレジスタ１１４のゲートパルス出力が各画素のＴＦＴスイッチ１０２のゲートに到達するまでに波形の鈍化が生じる。この鈍化はシフトレジスタ１１４から離れる程大きくなる。さらに画面が大型化すると、ゲート線１１１自身の寄生抵抗、寄生容量も大きくなり、さらにこの鈍化が大きくなる。

【０００９】各画素に高解像度の表示入力を与えるためには、信号線出力が安定化してからゲートパルスを加えてゲートを開く必要があるが、上記信号線出力の過渡時間とゲートパルスの鈍化により前記従来技術によるマトリクス型画像表示装置では、上記１６．３μｓ以下でこれを実現することが困難になる。

【００１０】

【発明が解決しようとする課題】本発明の目的は、上記従来技術の問題点を解消し、短い表示信号入力時間の間でも各画素に高解像度の表示信号を入力可能とするマトリクス型画像表示装置を提供することにある。

【００１１】本発明の他の目的は、大画面でも、動画の動きが滑らかで、各画素に高解像度の表示信号を入力可能とするマトリクス型画像表示装置を提供することにある。

【００１２】本発明の別の目的は、簡潔なプロセス技術により製作可能なマトリクス型画像表示装置を提供することにある。

【００１３】さらに、本発明の別の目的は、表示画面内に装置の主要部または全部を作り込んだ、いわゆる、システム　イン　ディスプレイを可能とするマトリクス型画像表示装置を提供することにある。

【００１４】

【課題を解決するための手段】上記目的を達成するための本発明の一つの基本的な特徴は、マトリクス型画像表示装置の各交点にある画像表示素子回路をデジタル画像信号により駆動するようにしたことである。

【００１５】上記目的を達成するための本発明の他の基本的な特徴は、マトリクス型画像表示装置の各交点マトリクス型にある画像表示素子回路が、ＤＡ変換器を備えていることである。

【００１６】上記目的を達成するための本発明の他の基本的な特徴は、マトリクス型画像表示装置の各交点にある画像表示素子回路が、ラッチとＤＡ変換器とを備えていることである。

【００１７】上記目的を達成するための本発明の別の基本的な特徴は、マトリクス型画像表示装置の各交点にある画像表示素子回路が、ＣＭＯＳで構成されたＤＡ変換器を備えていることである。

【００１８】上記目的を達成するため、本発明のマトリクス型画像表示装置では、列方向に各画素を接続する信号線１１２にＤＡ変換器１１６出力のアナログ信号を供給する代わりに、列方向に各画素を接続するデータバスを設け、このデータバスにデジタル表示データを供給する。そして各画素内にＤＡ変換器を設け、各画素内でアナログデータに変換し、液晶静電容量を駆動する。この際、ＤＡ変換器とデータバスの間にラッチを設けることにより、データの正確なタイミングでの取り込みを実現することができる。

【００１９】

【発明の実施の形態】本発明のマトリクス型画像表示装置の実施の形態を図により説明する。

【００２０】図1において、１３は、ガラス基板で、ガ

ラス基板１３の上には、各々がゲート線１１及びデータバス１２に接続された、多数の表示画素回路１４がマトリクス状に形成されている。

【００２１】各表示画素回路１４に対応して、透過光量を変調するためのＴＮ液晶層が設けられているが、これを静電容量２３で示している。静電容量２３の一方の電極には８ビットのＤＡ変換器２２の出力が接続されている。ＤＡ変換器２２の入力には、８ビットのラッチ２１の出力が接続されている。ラッチ２１のタイミング入力はゲート線１１を介して、Ｙ駆動回路１５に接続されている。また、ラッチ２１のデータ入力は、８ビットのデータバス１２を介してＸ駆動回路１６に接続されている。Ｙ駆動回路１５とＸ駆動回路１６とは、ともに制御回路１９に接続され、制御回路１９には信号入力端子２０が設けられている。また、ＴＮ液晶静電容量２３の他方の電極は、共通電極２４に接続されている。

【００２２】Ｙ駆動回路１５は、制御回路１９から入力されるクロック１７に従い、各行のゲート線１１を順次選択して高電圧レベルに設定する。Ｘ駆動回路１６にはデジタル表示信号がデジタル入力線１８を経由して入力されており、一行分のデジタル表示信号が揃った時点で、各列毎に８ビットデータバス１２に出力される。なお画素にラッチを用いた場合、メモリ効果があるためフレームレートが低減できる、さらにＹ駆動回路１５は選択的に書き込むことができるという利点がある。

【００２３】第０番目から第Ｍ－１番目までの各ゲート線１１上のゲート信号Ｙ０、Ｙ１、…ＹＭ－１及び第０番目から第Ｎ－１番目までの各８ビットデータバス１２上のデジタル表示データＸ０、Ｘ１、…ＸＮ－１の変化のタイミングを図２に示す。ここで、Ｎ、Ｍの実際の値は画素数１２８０×１０２４のカラー表示装置では、Ｍ＝１０２４、Ｎ＝１２８０×３になる。図２のタイムチャートにおいて、１フレーム＝１／６０秒とした。Ｍ行の画素の値の入力データの更新が、１フレームを周期として一巡して完了する。ゲート信号とデジタル表示データの位相は、ずれており、デジタル表示データが確定したタイミングでデジタル表示データを８ビットのラッチ２１に取り込むようになっている。

【００２４】８ビットのラッチ２１は、クロック同期（Ｃｌｏｃｋｅｄ）インバータを用いたＣＭＯＳ論理によって、図３のように構成する。図３（ａ）は記号表示、図３（ｂ）はゲート表示で表わした８ビットラッチ２１である。

【００２５】図４は、Ｃｌｏｃｋｅｄ　インバータ自身の詳細な回路図を示す。図４（ａ）は記号表示、図４（ｂ）はゲート表示で表わしたＣｌｏｃｋｅｄ　インバータ２１である。図４（ｂ）に示すように、各Ｃｌｏｃｋｅｄ　インバータは４つのＣＭＯＳトランジスタからなり、薄膜のＰｏｌｙ－Ｓｉ、ａ－Ｓｉ、単結晶Ｓｉをチャネルに用いた薄膜トランジスタで構成することが望ましい。

【００２６】前述したように、Ｍ＝１０２４とすると、図２における、１行あたりの表示信号入力時間Ｔｉｎは、１／６０÷１０２４＝１６．３μｓの半周期以下である。しかし、ラッチ２１が取り込むのはデジタル信号であるから、Ｔｉｎの後端でデータバス１２の各ビット線の値がＣＭＯＳの論理しきい値を超えていれば、’０’又は’１’の判定が正しくできる。このため１本の信号線に８ビット精度（２５６階調）のアナログ信号を通す場合よりも容易に正確な信号値の判別が可能である。なお、データバス１２には８ビットのパラレルのビット線を用いたが、シリアルでもよい。

【００２７】８ビットのＤＡ変換器２２の構成を図５に示す。図５（ａ）は記号表示、図５（ｂ）はゲート表示で表わしたＤＡ変換器２２である。図５（ｂ）において、Ｄ７を入力とするＭＳＢ部からＤ０を入力とするＬＳＢ部までの８段で８ビットＤＡ変換器が実現される。図５（ｂ）では、図面の簡潔化のために、Ｄ７を入力とするＭＳＢ部対応の１段のＤＡ変換器４１のみ詳細な回路を示し、他のＤＡ変換器は、ＤＡ変換器４１とまったく同様の構成なので、単にボックスで示す。図５のＤＡ変換器４１は電流切替型として知られている形式である。

【００２８】このＤＡ変換器は入力信号以外のクロックを必要とせず、ＤＡ変換器１段が１６個のＭＯＳトランジスタのみで実現でき、抵抗や容量等の受動素子が不要なことから高集積化に適する。またプロセス的にも（液晶層静電容量以外の）容量形成工程が不要であることから、低コスト化に適する。なお、ＤＡ変換器を構成するデバイスは、薄膜のＰｏｌｙ－Ｓｉ、ａ－Ｓｉ、単結晶Ｓｉをチャネルに用いた薄膜トランジスタで構成することが望ましい。４２、４３は正負の出力電流線、４４は出力電流を電圧に変換する電流－電圧変換器である。電流－電圧変換器はオペアンプ４５を含む。

【００２９】オペアンプ４５の構成を図６に示す。図６（ａ）は記号表示、図６（ｂ）はゲート表示で表わしたオペアンプ４５である。同図で、基本部分はＶｉｎ１、Ｖｉｎ２の差動入力に対し、Ｖｏｕｔ１、Ｖｏｕｔ２の差動出力を出力する。ＶＣＭ、ＶＢＮは基本部分の動作に必要なバイアス電圧であり、図７に示すバイアス電圧発生回路により生成される。なお、オペアンプを構成するデバイスも、薄膜のＰｏｌｙ－Ｓｉ、ａ－Ｓｉ、単結晶Ｓｉをチャネルに用いた薄膜トランジスタで構成することが望ましい。

【００３０】以上の回路構成から明らかなように、本発明の各画像表示素子回路は、ラッチ及びＤＡ変換器からなるが、回路規模的には、ＤＡ変換器が大部分を占める。したがって、ＤＡ変換器の形成プロセス及び構成規模が重要となる。本発明では、ＤＡ変換器をはじめ、ラッチ、オペアンプなどの全てのあるいは主要な回路をＣ

MOSプロセスで形成することにより所期の目的を達成することができる。すなわち、図4のラッチ回路、図5のDA変換器回路、図6のオペアンプ、及び、図7のバイアス電圧発生回路のいずれの回路もCMOSトランジスタにより構成されている。

【0031】図8は、薄膜トランジスタから構成されるCMOS（相補型トランジスタ）の断面構造を示す。図において、ガラスや石英などの絶縁性基板81上の多結晶シリコン層80に、n型チャネルTFT90とp型チャネルTFT91とからなるCMOS薄膜トランジスタを構成する。薄膜トランジスタのチャネルには薄膜のポリシリコン層80からなる薄膜を用いているが、a－Si薄膜、単結晶Si薄膜を用いても同様である。n型チャネルTFT90はポリシリコン層80にn型のソース拡散層88とそれと接続したソース電極85、n型のドレイン拡散層89とそれと接続したドレイン電極84、さらにゲート絶縁膜86を介してゲート電極87を設置することにより電界効果型トランジスタとして動作する。同様にp型チャネルTFT91は多結晶シリコン層88とそれと接続したソース電極85、p型のドレイン拡散層89とそれと接続したドレイン電極84、さらにゲート絶縁膜86を介してゲート電極88を設置することにより電界効果型トランジスタとして動作する。

【0032】上記の構造のCMOSトランジスタで形成すれば、図5のDA変換器の占有面積は、例えば、0.25μmのサブミクロン技術を用いれば、図4の8ビットのラッチを合わせても、100μm×100μmの大きさの面積に収めることが可能である。この大きさは例えば28インチのSXGA型（1280×1024画素）のカラー大型表示素子においては開口率を16%減少するだけであり、十分実用に耐え得るものである。さらに、0.15のサブミクロン技術プロセスを用いれば、開口率の減少は、5%程度となり、ほとんど問題とならない。

【0033】図9に画像装置の全体構成を示す。2枚のガラス板102、103を数μmの空間105を介して対向させ固定し、その間に液晶100を封入した構造となっている。上部ガラス基板102上には、共通電極とカラーフィルタの他に、本発明により、列対応に設けたデータバス、並びに、各画素対応のラッチ、DA変換器を含む画像表示素子回路が全て形成された画像表示回路104が配置されている。これらを2枚の偏光板101で挟み、図9の下方から、白色光を入射させると透過型の表示装置となる。

【0034】さらに、図9の表示装置に、図1に示す制御回路並びにX駆動回路及びY駆動回路も作り込むことができ、いわゆる、システム　イン　ディスプレイとすることもできる。

【0035】なお、本実施の形態では、電流切替型のDA変換器を用いたが、これに代えて抵抗から構成される抵抗分割型、あるいは容量分割型で構成しても同様の効果が得られる。

【0036】

【発明の効果】以上説明したように、本発明によれば、各画素にデジタル表示データを伝送すればよいので、短い表示信号入力時間の間でも各画素に高解像度の表示信号を入力するができ、高解像度の表示素子を実現することができる。

【図面の簡単な説明】

【図1】本発明による画像表示装置の一実施の形態を示す回路構成図。

【図2】図1の動作を説明するための信号変化を示すタイミング図。

【図3】図1のラッチの記号表示回路構成図（a）及びゲート表示回路構成図（b）。

【図4】図1のインバータの記号表示回路構成図（a）及びゲート表示回路構成図（b）。

【図5】図1のDA変換器の記号表示回路構成図（a）及びゲート表示回路構成図（b）。

【図6】図1のオペアンプの記号表示回路構成図（a）及びゲート表示回路構成図（b）。

【図7】図1のオペアンプ用のバイアス電圧発生回路のゲート表示回路構成図。

【図8】図1の画像表示装置の回路形成部を示す断面図。

【図9】図1の画像表示装置の全体構成を示す分解斜視図。

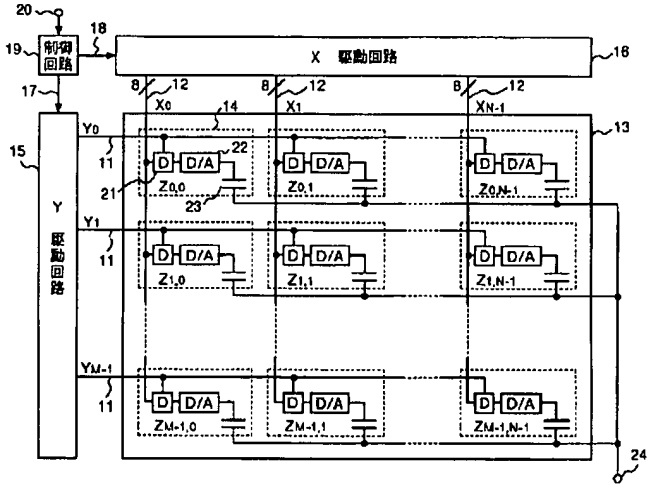
【図10】従来の画像表示装置の回路構成図。

【符号の説明】

14…表示画素、23…TN液晶層静電容量、22…DA変換器、21…ラッチ、11…ゲート線、15…Y駆動回路、12…データバス、16…X駆動回路、19…制御回路、20…信号入力端子、24…共通電極、17…クロック、18…デジタル入力線、41…MSBのDA変換器、42、43…正負の出力電流線、44…電流ー電圧変換器、45…オペアンプ、80…多結晶シリコン層、81…絶縁性基板、83…チャネル形成領域、84…ドレイン電極、85…ソース電極、86…ゲート絶縁膜、87…ゲート電極、88…ドレイン拡散層、89…ソース拡散層、90…n型チャネルTFT、91…p型チャネルTFT、100…画像表示素子、101…偏光板、102…下部ガラス基板、103…上部ガラス基板、104…カラーフィルタ、105…液晶

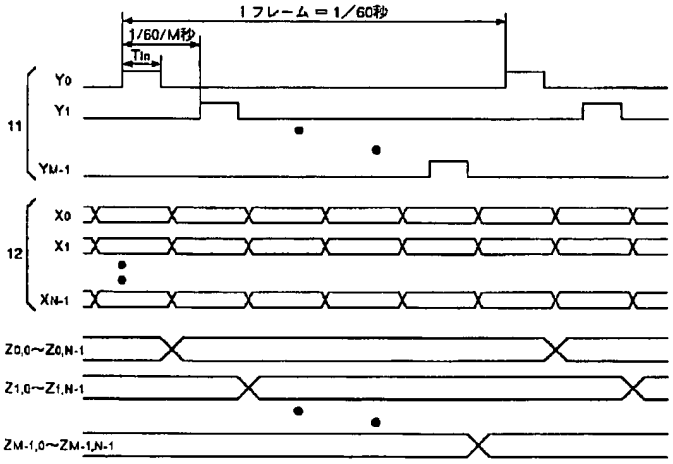
【図1】

図 1



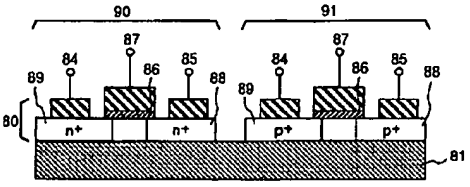

【図2】

図 2



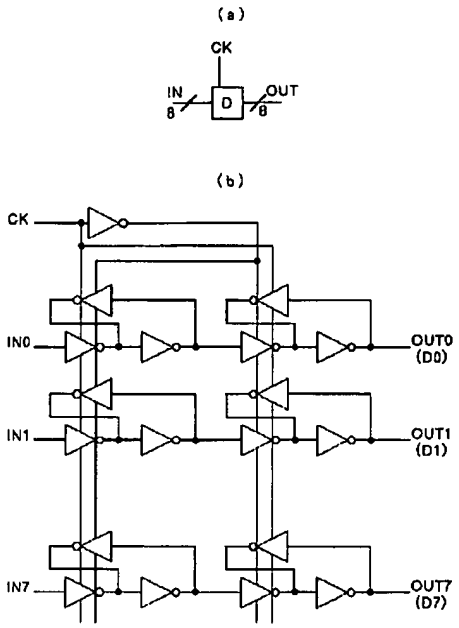

【図8】

図 8



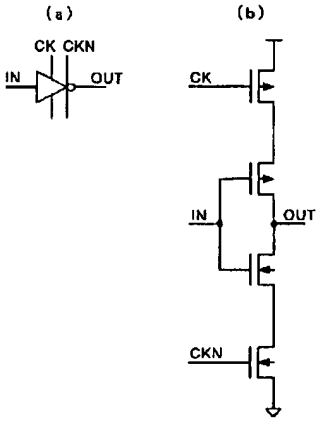

【図3】

図 3



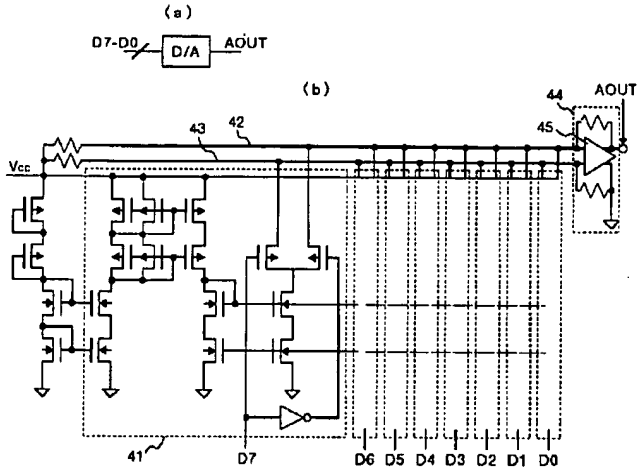

【図4】

図 4



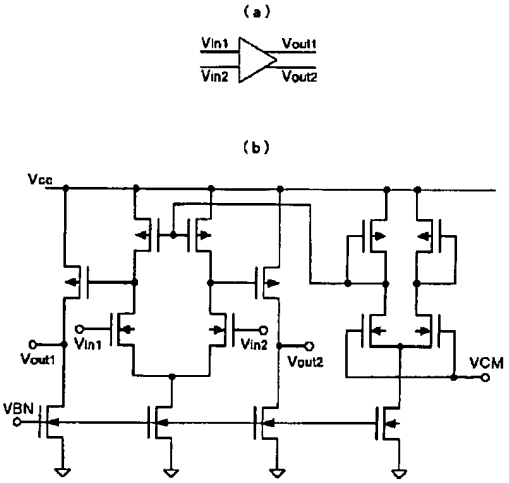
【図5】

図 5



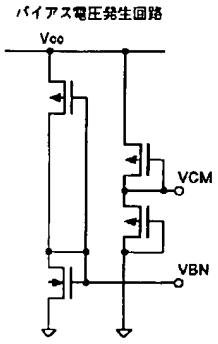

【図6】

図 6



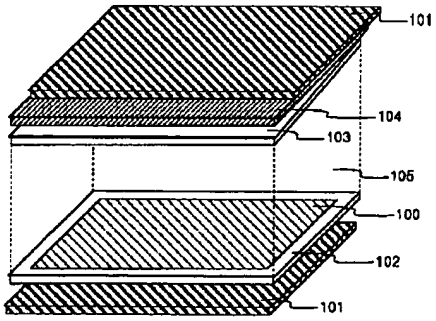

【図7】

図 7



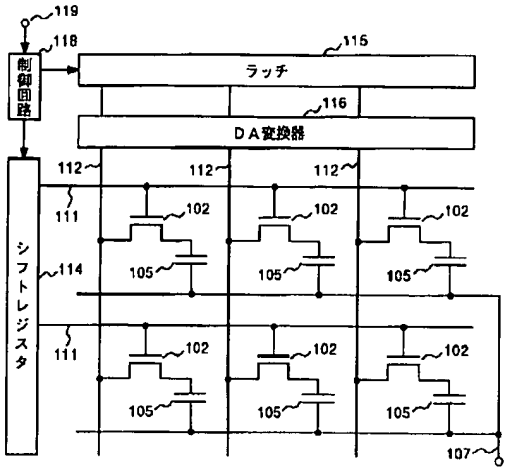

【図9】

図 9



【図10】

図 10


119
118
制御回路
115
ラッチ
116
DA変換器
112
112
112
111
102
102
102
105
105
105
114
シフトレジスタ
111
102
102
102
105
105
105
107

# PATENT ABSTRACTS OF JAPAN

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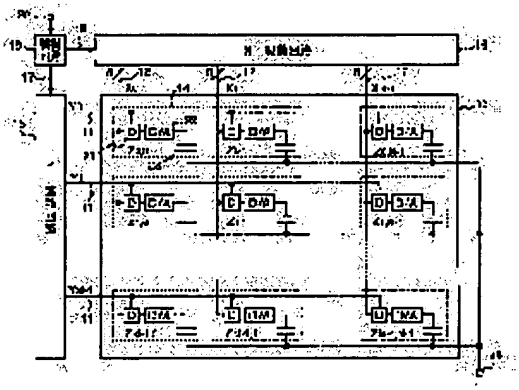
AKIMOTO HAJIME
NAKAHARA HITOSHI

## (54) MATRIX TYPE IMAGE DISPLAY DEVICE

(57) Abstract:
PROBLEM TO BE SOLVED: To provide a high resolution and large-sized matrix type display device capable of inputting a high resolution display signal to respective pixels even during a short display signal input time.
SOLUTION: Each display pixel circuit 14 is provided with a D/A converter 22, and a TN liquid crystal capacitor 23 is connected to the output of the D/A converter 22, and the output of a latch is connected to the input. The timing input of the latch 21 is connected to a Y drive circuit 15 through a gate line 11, and the data input of the latch 21 is connected to an X drive circuit 16 through a data bus 12. The other end of the TN capacitor 23 is connected to a common electrode 24. The Y drive circuit 15 selects successively the gate line of respective rows according to a clock 17 inputted from a control circuit 19 to set it in a high voltage level. A digital display signal is inputted to the X drive circuit 16 through a digital input line 18, and to be outputted to the data bus 12 at every row when digital display signals by one row are collected.



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rejection or application converted registration]

[Date of final disposal for application]

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[Date of registration]

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[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] It is the matrix type image display equipment characterized by being the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, and two or more aforementioned image display element circuits having a DA converter respectively.
[Claim 2] The image display element circuit which is the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, and two or more aforementioned image display element circuits have in each intersection of matrix type image display equipment respectively is the matrix type image display equipment characterized by having the latch and the DA converter.
[Claim 3] It is equipping [ are the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, and / two or more aforementioned image display element circuits / with the DA converter which consisted of CMOS respectively ] matrix type image display equipment.
[Claim 4] Matrix type image display equipment which is the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, and is respectively characterized by giving a picture signal in the form of a digital signal in two or more aforementioned image display element circuits.
[Claim 5] Matrix type image display equipment characterized by being the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, preparing the data bus which connects each image display element circuit in the orientation of a train, preparing a DA converter in each image display element circuit, and changing into analog data in each image display element circuit.
[Claim 6] Matrix type image display equipment characterized by being the matrix type image display equipment which consists of a glass substrate and two or more image display element circuits which arrange 2-dimensional in the shape of a matrix, and were formed on this glass substrate, having prepared the data bus which connects each image display element circuit in the orientation of a train, having prepared the DA converter in each image display element circuit, and preparing a latch between the aforementioned DA converter and a data bus further.
[Claim 7] The latch and DA converter which were prepared corresponding to each of a pixel electrode and two or more aforementioned display pixel electrodes are included. It connects with the gate line which supplies the signal with which the timing input of the aforementioned latch scans two or more aforementioned display pixel electrodes per line. The data input of the aforementioned latch is connected to the data bus which supplies digital display data to two or more aforementioned display

pixel electrodes per train. Matrix type image display equipment characterized by connecting the data output of the aforementioned latch to the input of the aforementioned DA converter, and connecting the output of the aforementioned DA converter to a display pixel electrode.
[Claim 8] The latch and DA converter which were prepared corresponding to each of two or more display pixel electrodes arranged 2-dimensional in the shape of a matrix and two or more aforementioned display pixel electrodes are included. It connects with the gate line which supplies the signal with which the timing input of the aforementioned latch scans two or more aforementioned display pixel electrodes per line. The data input of a latch is connected to the data bus which supplies digital display data to two or more aforementioned display pixel electrodes per train. Matrix type image display equipment characterized by connecting the data output of the aforementioned latch to the input of the aforementioned DA converter, and connecting the output of the aforementioned DA converter to a display pixel electrode.
[Claim 9] Matrix type image display equipment according to claim 7 characterized by being formed on two or more aforementioned display pixel electrodes, two or more aforementioned latches, two or more aforementioned DA converters, two or more aforementioned gate lines, and the glass substrate of the couple to which two or more aforementioned data buses pinch a liquid crystal layer.
[Claim 10] Two or more aforementioned latches are Clocked which consisted of CMOS. Image display equipment according to claim 7 characterized by consisting of an inverter.
[Claim 11] Two or more aforementioned DA converters are matrix type image display equipment according to claim 7 characterized by consisting of the current change type which consisted of CMOS.
[Claim 12] Two or more aforementioned latches and two or more aforementioned DA converters are matrix type image display equipment according to claim 7 currently formed on the glass substrate of the couple which consists of TFT and pinches a liquid crystal layer.

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* NOTICES *



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3.In the drawings, any words are not translated.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to matrix type image display equipment, especially the matrix type image display equipment which enables a high-resolution display on a large-sized screen.
[0002]
[Description of the Prior Art] As conventional matrix type image display equipment, liquid crystal image display equipment is taken for an example, and is explained using drawing 10 . Drawing 10 is a block diagram of the liquid crystal image display equipment by the proior art. As an example of such conventional image display equipment, it is SID94, for example. Digest of Technical Papers, pp.359-362 etc. are known (1994).
[0003] In drawing 10 , although TN (Twisted Nematic) liquid crystal layer for modulating the amount of transmitted lights is prepared in each pixel (image display element) which has more than one in the intersection of the gate line 111 of a book, and the signal line 112 respectively, electrostatic capacity 105 shows this. Each image display element circuit, the configuration of the drive circuit, and an operation are as follows.
[0004] The TFT (Thin Film Transistor) switch 102 is connected to electrostatic capacity 105. The gate of the TFT switch 102 is connected to the shift register 114 through the gate line 111. Moreover, the drain of the TFT switch 102 is connected to the latch circuit 115 through the signal line 112 and DA converter 116. Both the shift register 114 and the latch circuit 115 are connected to a control circuit 118, and the signal input terminal 119 is formed in the control circuit 118. In addition, the other end of TN liquid crystal electrostatic capacity 105 is connected to the common electrode 107.
[0005] According to the clock inputted from a control circuit 118, a shift register 114 chooses the gate line 111 one by one, and sets it as high-voltage level. The status signal for one line is inputted into the latch circuit 115, and this status signal is inputted into a signal line 112 through DA converter 116. Since the TFT switch 102 of the line chosen through the gate line 111 by the shift register 114 is turned on, a status signal is inputted into TN liquid crystal electrostatic capacity 105 of the selected line through a signal line 112. Since the optical property is controlled by applied voltage, TN liquid crystal can display image information on a display pixel matrix by combining with the polarizing plate and back light which are omitted all over drawing.
[0006] In image display equipment, in order to make a motion of an animation smooth visually, generally it is required to make an inter-frame display interval into 1 / 60 seconds or less. For that, it is necessary to input a status signal within 1 / 60 seconds to all display pixels. On the other hand, with SXGA type image display equipment which are a high resolution and the example of representation of the matrix type image display equipment of ********, the number of pixels is 1280x1024 pixels, and a line count is 1024. For this reason, the status-signal input time per line is less than [ 1/60/1024=16.3microsecond ] securable.
[0007] However, by the time its output is stable however a signal line 112 may make the output

impedance of DA converter 116 small since it has parasitism resistance and a parasitic capacitance, the transition duration is required for it with the matrix type image display equipment by the above-mentioned conventional technique. This transition duration becomes so large that it separates from DA converter 116. If a screen large-sized-izes, this transition duration will become large further.
[0008] On the other hand, the TFT switch 102 which one gate line 111 drives becomes about 1280 with the image display equipment of SXGA type (1280x1024 pixels) high resolution. In the thing of the color, it increases these 3 times. For this reason, the load capacity connected to the gate line 111 becomes large with the image display equipment of a high resolution. For this reason, however it may make the output impedance of a shift register 114 small, by the time the gate pulse output of a shift register 114 arrives at the gate of the TFT switch 102 which is each pixel, wave-like slowdown will arise. This slowdown becomes so large that it separates from a shift register 114. If a screen furthermore large-sized-izes, parasitism resistance of gate line 111 self and a parasitic capacitance will also become large, and this slowdown will become large further.
[0009] Although it is necessary to add a gate pulse and to open the gate after a signal-line output is stable in order to give the display input of a high resolution to each pixel, it becomes difficult to realize this in the 16.3 or less above-mentioned microseconds with the matrix type image display equipment by the aforementioned conventional technique by the transition duration of the above-mentioned signal-line output and slowdown of a gate pulse.
[0010]
[Problem(s) to be Solved by the Invention] The purpose of this invention cancels the trouble of the above-mentioned conventional technique, and is to offer the matrix type image display equipment which enables the input of the status signal of a high resolution also between short status-signal input time at each pixel.
[0011] Also by the big screen, other purposes of this invention have a smooth motion of an animation, and are to offer the matrix type image display equipment which enables the input of the status signal of a high resolution at each pixel.
[0012] Another purpose of this invention is to offer the matrix type image display equipment which can be manufactured with brief process technique.
[0013] Furthermore, another purpose of this invention is the so-called system which made the principal part or all of equipment in the display screen. Inn It is in offering the matrix type image display equipment which makes a display possible.
[0014]
[Means for Solving the Problem] One fundamental characteristic feature of this invention for attaining the above-mentioned purpose is having been made to drive the image display element circuit in each intersection of matrix type image display equipment according to a digital picture signal.
[0015] Other fundamental characteristic features of this invention for attaining the above-mentioned purpose are that the image display element circuit in each intersection matrix type of matrix type image display equipment is equipped with a DA converter.
[0016] Other fundamental characteristic features of this invention for attaining the above-mentioned purpose are that the image display element circuit in each intersection of matrix type image display equipment is equipped with a latch and a DA converter.
[0017] Another fundamental characteristic feature of this invention for attaining the above-mentioned purpose is that the image display element circuit in each intersection of matrix type image display equipment is equipped with the DA converter which consisted of CMOS.
[0018] In order to attain the above-mentioned purpose, with the matrix type image display equipment of this invention, instead of supplying the analog signal of DA converter 116 output in the orientation of a train at the signal line 112 which connects each pixel, the data bus which connects each pixel is prepared in the orientation of a train, and digital display data are supplied to this data bus. And a DA converter is prepared in each pixel, it changes into analog data within each pixel, and liquid crystal electrostatic capacity is driven. In this case, the incorporation by the exact timing of data is realizable by preparing a latch between a DA converter and a data bus.

[0019]
[Embodiments of the Invention] Drawing explains the gestalt of implementation of the matrix type image display equipment of this invention.
[0020] In drawing 1 , 13 is a glass substrate and many display pixel circuits 14 where each was connected to the gate line 11 and the data bus 12 are formed in the shape of a matrix on the glass substrate 13.
[0021] Although TN liquid crystal layer for modulating the amount of transmitted lights is prepared corresponding to each display pixel circuit 14, electrostatic capacity 23 shows this. The output of 8-bit DA converter 22 is connected to one electrode of electrostatic capacity 23. The output of the 8-bit latch 21 is connected to the input of DA converter 22. The timing input of latch 21 is connected to Y drive circuit 15 through the gate line 11. Moreover, the data input of latch 21 is connected to X drive circuit 16 through the 8-bit data bus 12. Both Y drive circuit 15 and X drive circuit 16 are connected to a control circuit 19, and the signal input terminal 20 is formed in the control circuit 19. Moreover, the electrode of another side of TN liquid crystal electrostatic capacity 23 is connected to the common electrode 24.
[0022] According to the clock 17 inputted from a control circuit 19, Y drive circuit 15 chooses the gate line 11 of each line one by one, and sets it as high-voltage level. The digital display signal is inputted into X drive circuit 16 via the digital input line 18, and when the digital display signal for a party becomes complete, it is outputted to the 8 bit data bus 12 for every train. In addition, when a latch is used for a pixel, since there is a memory effect, Y drive circuit 15 has further the advantage which can reduce frame rate that it can write in alternatively.
[0023] The gate signals Y0 and Y1 on each gate line 11 from the 0th to the M-1st, the digital display data X0 and X1 on --YM-1 and the 8 bit each data buses 12 from the 0th to the N-1st, and the timing of change of --XN-1 are shown in drawing 2 . Here, the actual value of N and M is set to M= 1024 and N= 1280x3 by the electrochromatic display with 1280x1024 pixels. In the timing diagram of drawing 2 , they could be one frame =1 / 60 seconds. The update of the input data of the value of the pixel of M lines takes a round of one frame as a period, and is completed. The phase of a gate signal and digital display data has shifted, and incorporates digital display data to the 8-bit latch 21 to the timing which digital display data decided.
[0024] CMOS logic which used the clock synchronization (Clocked) inverter constitutes the 8-bit latch 21, as shown in drawing 3 . It is the 8 bit latch 21 which drawing 3 (a) expressed with the notation display, and drawing 3 (b) expressed with the gate display.
[0025] Drawing 4 is Clocked. The own detailed circuit diagram of an inverter is shown. It is Clocked which drawing 4 (a) expressed with the notation display, and drawing 4 (b) expressed with the gate display. It is an inverter 21. It is each Clocked as shown in drawing 4 (b). As for an inverter, it is desirable to constitute from the TFT which consisted of four CMOS transistors and used Poly-Si of a thin film, a-Si, and single crystal Si for the channel.
[0026] As mentioned above, when M= 1024, the status-signal input time Tin per line in drawing 2 is below a 1/60/1024=16.3microsecond half period. However, that latch 21 incorporates can perform a judgment of '0' or '1' correctly, if the value of each bit line of a data bus 12 is over the logic threshold of CMOS by the back end of Tin, since it is a digital signal. For this reason, distinction of an exact signal value is more easily [ than the case where it lets the analog signal of 8 bit precision (256 gradation) pass to one signal line ] possible. In addition, although the 8-bit parallel bit line was used for the data bus 12, it is good even when it is serial.
[0027] The configuration of 8-bit DA converter 22 is shown in drawing 5 . It is DA converter 22 which drawing 5 (a) expressed with the notation display, and drawing 5 (b) expressed with the gate display. In drawing 5 (b), a 8 bit DA converter is realized in eight steps to LSB section which considers D0 as an input from MSB section which considers D7 as an input. With drawing 5 (b), one card row of MSB section correspondence which considers D7 as an input for brief-izing of a drawing accepts it DA converter 41, a detailed circuit is shown, and since other DA converters are the completely same configurations as DA converter 41, with it, they are only shown with a box. DA converter 41 of drawing

5 is a format known as a current change type.
[0028] A clock except an input signal is not needed, but one step of DA converter can be realized only by 16 MOS transistors, and since passive elements, such as resistance and capacity, are unnecessary, this DA converter is suitable for high integration. Moreover, since the capacity formation process (except for liquid crystal layer electrostatic capacity) is unnecessary also in process, it is suitable for low-cost-ization. In addition, as for the device which constitutes a DA converter, it is desirable to constitute Poly-Si of a thin film, a-Si, and single crystal Si from the TFT used for the channel. It is the current-voltage converter from which change 42 and 43 into the output current line of positive/negative, and 44 changes the output current into a voltage. A current-voltage converter contains an operational amplifier 45.
[0029] The configuration of an operational amplifier 45 is shown in drawing 6 . It is the operational amplifier 45 which drawing 6 (a) expressed with the notation display, and drawing 6 (b) expressed with the gate display. In this drawing, a basic fraction outputs the differential output of Vout1 and Vout2 to the difference input of Vin1 and Vin2. VCMVBN is bias voltage required for an operation of a basic fraction, and is generated by the bias voltage occurrence circuit shown in drawing 7 . In addition, it is desirable to also constitute the device which constitutes an operational amplifier from the TFT which used Poly-Si of a thin film, a-Si, and single crystal Si for the channel.
[0030] Although each image display element circuit of this invention consists of a latch and a DA converter, a DA converter occupies most in circuit scale, so that clearly from the above circuit arrangement. Therefore, the formation process and configuration scale of a DA converter become important. this invention -- a DA converter -- beginning -- a latch, an operational amplifier, etc. -- all -- it is -- it is -- the desired end can be attained by forming main circuits by the CMOS process That is, the latch circuit of drawing 4 , the DA converter circuit of drawing 5 , the operational amplifier of drawing 6 , and any circuit of the bias voltage occurrence circuit of drawing 7 are constituted by CMOS transistor.
[0031] Drawing 8 shows the cross-section structure of CMOS (complementary transistor) which consists of TFT. In drawing, CMOS TFT which becomes the polycrystal silicon layer 80 on the insulating substrates 81, such as glass and a quartz, from n type channel TFT90 and p type channel TFT91 is constituted. Although the thin film which consists of a polysilicon contest layer 80 of a thin film is used for the channel of TFT, it is the same even if it uses an a-Si thin film and a single crystal Si thin film. N type channel TFT90 operates as a field effect transistor the source electrode 85 which connected with the n type source diffusion layer 88 and it at the polysilicon contest layer 80, the drain electrode 84 which connected with the n type drain diffusion layer 89 and it, and by installing the gate electrode 87 through the gate insulator layer 86 further. p type channel TFT91 operates as a field effect transistor similarly the source electrode 85 linked to the polycrystal silicon layer 88 and it, the drain electrode 84 linked to the p type drain diffusion layer 89 and it, and by installing the gate electrode 88 through the gate insulator layer 86 further.
[0032] If it forms with CMOS transistor of the above-mentioned structure, the occupancy area of the DA converter of drawing 5 can be stored in the area of a 100micrometerx100micrometer size, even if it doubles a 8-bit latch of drawing 4 , if 0.25-micrometer submicron technique is used. In a 28 inches SXGA type (1280x1024 pixels) color large-sized display device, as for this size, decreasing 16% can only bear a numerical aperture enough at practical use. Furthermore, if the submicron technical process of 0.15 is used, the decrement in a numerical aperture will become about 5%, and will hardly pose a problem.
[0033] The whole picture image equipment configuration is shown in drawing 9 . The glass plates 102 and 103 of two sheets are made to counter through the micrometers [ several ] space 105, and it fixes, and has the structure which enclosed liquid crystal 100 between them. The image display circuit 104 where all the image display element circuits that contain the data bus prepared in train correspondence and a latch of each pixel correspondence, and a DA converter by this invention other than a common electrode and a light filter were formed on the up glass substrate 102 is arranged. These are inserted with two polarizing plates 101, and if incidence of the white light is carried out, it will become penetrated type display from the lower part of drawing 9 .

[0034] Furthermore, the control circuit, X drive circuit, and Y drive circuit which are shown in the display of drawing 9 in drawing 1 can also be made, and it is the so-called system. Inn It can also consider as a display.

[0035] In addition, with the gestalt of this operation, although the current change type DA converter was used, even if it constitutes from a resistance assembled die which replaces with this and consists of resistance, or a capacitive component split mold, the same effect is acquired.

[0036]

[Effect of the Invention] It can do, although the status signal of a high resolution is inputted into each pixel also between short status-signal input time according to this invention since what is necessary is just to transmit digital display data to each pixel, as explained above, and the display device of a high resolution can be realized.

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[Translation done.]

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Technique

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[Description of the Prior Art] As conventional matrix type image display equipment, liquid crystal image display equipment is taken for an example, and is explained using drawing 10 . Drawing 10 is a block diagram of the liquid crystal image display equipment by the proior art. As an example of such conventional image display equipment, it is SID94, for example. Digest of Technical Papers, pp.359-362 etc. are known (1994).
[0003] In drawing 10 , although TN (Twisted Nematic) liquid crystal layer for modulating the amount of transmitted lights is prepared in each pixel (image display element) which has more than one in the intersection of the gate line 111 of a book, and the signal line 112 respectively, electrostatic capacity 105 shows this. Each image display element circuit, the configuration of the drive circuit, and an operation are as follows.
[0004] The TFT (Thin Film Transistor) switch 102 is connected to electrostatic capacity 105. The gate of the TFT switch 102 is connected to the shift register 114 through the gate line 111. Moreover, the drain of the TFT switch 102 is connected to the latch circuit 115 through the signal line 112 and DA converter 116. Both the shift register 114 and the latch circuit 115 are connected to a control circuit 118, and the signal input terminal 119 is formed in the control circuit 118. In addition, the other end of TN liquid crystal electrostatic capacity 105 is connected to the common electrode 107.
[0005] According to the clock inputted from a control circuit 118, a shift register 114 chooses the gate line 111 one by one, and sets it as high-voltage level. The status signal for one line is inputted into the latch circuit 115, and this status signal is inputted into a signal line 112 through DA converter 116. Since the TFT switch 102 of the line chosen through the gate line 111 by the shift register 114 is turned on, a status signal is inputted into TN liquid crystal electrostatic capacity 105 of the selected line through a signal line 112. Since the optical property is controlled by applied voltage, TN liquid crystal can display image information on a display pixel matrix by combining with the polarizing plate and back light which are omitted all over drawing.
[0006] In image display equipment, in order to make a motion of an animation smooth visually, generally it is required to make an inter-frame display interval into 1 / 60 seconds or less. For that, it is necessary to input a status signal within 1 / 60 seconds to all display pixels. On the other hand, with SXGA type image display equipment which are a high resolution and the example of representation of the matrix type image display equipment of ********, the number of pixels is 1280x1024 pixels, and a line count is 1024. For this reason, the status-signal input time per line is less than [ 1/60/1024=16.3microsecond ] securable.
[0007] However, by the time its output is stable however a signal line 112 may make the output impedance of DA converter 116 small since it has parasitism resistance and a parasitic capacitance, the transition duration is required for it with the matrix type image display equipment by the above-mentioned conventional technique. This transition duration becomes so large that it separates from DA converter 116. If a screen large-sized-izes, this transition duration will become large further.
[0008] On the other hand, the TFT switch 102 which one gate line 111 drives becomes about 1280 with the image display equipment of SXGA type (1280x1024 pixels) high resolution. In the thing of the

color, it increases these 3 times. For this reason, the load capacity connected to the gate line 111 becomes large with the image display equipment of a high resolution. For this reason, however it may make the output impedance of a shift register 114 small, by the time the gate pulse output of a shift register 114 arrives at the gate of the TFT switch 102 which is each pixel, wave-like slowdown will arise. This slowdown becomes so large that it separates from a shift register 114. If a screen furthermore large-sized-izes, parasitism resistance of gate line 111 self and a parasitic capacitance will also become large, and this slowdown will become large further.

[0009] Although it is necessary to add a gate pulse and to open the gate after a signal-line output is stable in order to give the display input of a high resolution to each pixel, it becomes difficult to realize this in the 16.3 or less above-mentioned microseconds with the matrix type image display equipment by the aforementioned conventional technique by the transition duration of the above-mentioned signal-line output and slowdown of a gate pulse.

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TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] The purpose of this invention cancels the trouble of the above-mentioned conventional technique, and is to offer the matrix type image display equipment which enables the input of the status signal of a high resolution also between short status-signal input time at each pixel.
[0011] Also by the big screen, other purposes of this invention have a smooth motion of an animation, and are to offer the matrix type image display equipment which enables the input of the status signal of a high resolution at each pixel.
[0012] Another purpose of this invention is to offer the matrix type image display equipment which can be manufactured with brief process technique.
[0013] Furthermore, another purpose of this invention is the so-called system which made the principal part or all of equipment in the display screen. Inn It is in offering the matrix type image display equipment which makes a display possible.

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MEANS

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[Means for Solving the Problem] One fundamental characteristic feature of this invention for attaining the above-mentioned purpose is having been made to drive the image display element circuit in each intersection of matrix type image display equipment according to a digital picture signal.
[0015] Other fundamental characteristic features of this invention for attaining the above-mentioned purpose are that the image display element circuit in each intersection matrix type of matrix type image display equipment is equipped with a DA converter.
[0016] Other fundamental characteristic features of this invention for attaining the above-mentioned purpose are that the image display element circuit in each intersection of matrix type image display equipment is equipped with a latch and a DA converter.
[0017] Another fundamental characteristic feature of this invention for attaining the above-mentioned purpose is that the image display element circuit in each intersection of matrix type image display equipment is equipped with the DA converter which consisted of CMOS.
[0018] In order to attain the above-mentioned purpose, with the matrix type image display equipment of this invention, instead of supplying the analog signal of DA converter 116 output in the orientation of a train at the signal line 112 which connects each pixel, the data bus which connects each pixel is prepared in the orientation of a train, and digital display data are supplied to this data bus. And a DA converter is prepared in each pixel, it changes into analog data within each pixel, and liquid crystal electrostatic capacity is driven. In this case, the incorporation by the exact timing of data is realizable by preparing a latch between a DA converter and a data bus.
[0019]
[Embodiments of the Invention] Drawing explains the gestalt of implementation of the matrix type image display equipment of this invention.
[0020] In drawing 1 , 13 is a glass substrate and many display pixel circuits 14 where each was connected to the gate line 11 and the data bus 12 are formed in the shape of a matrix on the glass substrate 13.
[0021] Although TN liquid crystal layer for modulating the amount of transmitted lights is prepared corresponding to each display pixel circuit 14, electrostatic capacity 23 shows this. The output of 8-bit DA converter 22 is connected to one electrode of electrostatic capacity 23. The output of the 8-bit latch 21 is connected to the input of DA converter 22. The timing input of latch 21 is connected to Y drive circuit 15 through the gate line 11. Moreover, the data input of latch 21 is connected to X drive circuit 16 through the 8-bit data bus 12. Both Y drive circuit 15 and X drive circuit 16 are connected to a control circuit 19, and the signal input terminal 20 is formed in the control circuit 19. Moreover, the electrode of another side of TN liquid crystal electrostatic capacity 23 is connected to the common electrode 24.
[0022] According to the clock 17 inputted from a control circuit 19, Y drive circuit 15 chooses the gate line 11 of each line one by one, and sets it as high-voltage level. The digital display signal is inputted into X drive circuit 16 via the digital input line 18, and when the digital display signal for a party becomes complete, it is outputted to the 8 bit data bus 12 for every train. In addition, when a latch is

used for a pixel, since there is a memory effect, Y drive circuit 15 has further the advantage which can reduce frame rate that it can write in alternatively.

[0023] The gate signals Y0 and Y1 on each gate line 11 from the 0th to the M-1st, the digital display data X0 and X1 on --YM-1 and the 8 bit each data buses 12 from the 0th to the N-1st, and the timing of change of --XN-1 are shown in drawing 2 . Here, the actual value of N and M is set to M= 1024 and N= 1280x3 by the electrochromatic display with 1280x1024 pixels. In the timing diagram of drawing 2 , they could be one frame =1 / 60 seconds. The update of the input data of the value of the pixel of M lines takes a round of one frame as a period, and is completed. The phase of a gate signal and digital display data has shifted, and incorporates digital display data to the 8-bit latch 21 to the timing which digital display data decided.

[0024] CMOS logic which used the clock synchronization (Clocked) inverter constitutes the 8-bit latch 21, as shown in drawing 3 . It is the 8 bit latch 21 which drawing 3 (a) expressed with the notation display, and drawing 3 (b) expressed with the gate display.

[0025] Drawing 4 is Clocked. The own detailed circuit diagram of an inverter is shown. It is Clocked which drawing 4 (a) expressed with the notation display, and drawing 4 (b) expressed with the gate display. It is an inverter 21. It is each Clocked as shown in drawing 4 (b). As for an inverter, it is desirable to constitute from the TFT which consisted of four CMOS transistors and used Poly-Si of a thin film, a-Si, and single crystal Si for the channel.

[0026] As mentioned above, when M= 1024, the status-signal input time Tin per line in drawing 2 is below a 1/60/1024=16.3microsecond half period. However, that latch 21 incorporates can perform a judgment of '0' or '1' correctly, if the value of each bit line of a data bus 12 is over the logic threshold of CMOS by the back end of Tin, since it is a digital signal. For this reason, distinction of an exact signal value is more easily [ than the case where it lets the analog signal of 8 bit precision (256 gradation) pass to one signal line ] possible. In addition, although the 8-bit parallel bit line was used for the data bus 12, it is good even when it is serial.

[0027] The configuration of 8-bit DA converter 22 is shown in drawing 5 . It is DA converter 22 which drawing 5 (a) expressed with the notation display, and drawing 5 (b) expressed with the gate display. In drawing 5 (b), a 8 bit DA converter is realized in eight steps to LSB section which considers D0 as an input from MSB section which considers D7 as an input. With drawing 5 (b), one card row of MSB section correspondence which considers D7 as an input for brief-izing of a drawing accepts it DA converter 41, a detailed circuit is shown, and since other DA converters are the completely same configurations as DA converter 41, with it, they are only shown with a box. DA converter 41 of drawing 5 is a format known as a current change type.

[0028] A clock except an input signal is not needed, but one step of DA converter can be realized only by 16 MOS transistors, and since passive elements, such as resistance and capacity, are unnecessary, this DA converter is suitable for high integration. Moreover, since the capacity formation process (except for liquid crystal layer electrostatic capacity) is unnecessary also in process, it is suitable for low-cost-ization. In addition, as for the device which constitutes a DA converter, it is desirable to constitute Poly-Si of a thin film, a-Si, and single crystal Si from the TFT used for the channel. It is the current-voltage converter from which change 42 and 43 into the output current line of positive/negative, and 44 changes the output current into a voltage. A current-voltage converter contains an operational amplifier 45.

[0029] The configuration of an operational amplifier 45 is shown in drawing 6 . It is the operational amplifier 45 which drawing 6 (a) expressed with the notation display, and drawing 6 (b) expressed with the gate display. In this drawing, a basic fraction outputs the differential output of Vout1 and Vout2 to the difference input of Vin1 and Vin2. VCMVBN is bias voltage required for an operation of a basic fraction, and is generated by the bias voltage occurrence circuit shown in drawing 7 . In addition, it is desirable to also constitute the device which constitutes an operational amplifier from the TFT which used Poly-Si of a thin film, a-Si, and single crystal Si for the channel.

[0030] Although each image display element circuit of this invention consists of a latch and a DA converter, a DA converter occupies most in circuit scale, so that clearly from the above circuit arrangement. Therefore, the formation process and configuration scale of a DA converter become

important. this invention -- a DA converter -- beginning -- a latch, an operational amplifier, etc. -- all -- it is -- it is -- the desired end can be attained by forming main circuits by the CMOS process That is, the latch circuit of drawing 4 , the DA converter circuit of drawing 5 , the operational amplifier of drawing 6 , and any circuit of the bias voltage occurrence circuit of drawing 7 are constituted by CMOS transistor.

[0031] Drawing 8 shows the cross-section structure of CMOS (complementary transistor) which consists of TFT. In drawing, CMOS TFT which becomes the polycrystal silicon layer 80 on the insulating substrates 81, such as glass and a quartz, from n type channel TFT90 and p type channel TFT91 is constituted. Although the thin film which consists of a polysilicon contest layer 80 of a thin film is used for the channel of TFT, it is the same even if it uses an a-Si thin film and a single crystal Si thin film. N type channel TFT90 operates as a field effect transistor the source electrode 85 which connected with the n type source diffusion layer 88 and it at the polysilicon contest layer 80, the drain electrode 84 which connected with the n type drain diffusion layer 89 and it, and by installing the gate electrode 87 through the gate insulator layer 86 further. p type channel TFT91 operates as a field effect transistor similarly the source electrode 85 linked to the polycrystal silicon layer 88 and it, the drain electrode 84 linked to the p type drain diffusion layer 89 and it, and by installing the gate electrode 88 through the gate insulator layer 86 further.

[0032] If it forms with CMOS transistor of the above-mentioned structure, the occupancy area of the DA converter of drawing 5 can be stored in the area of a 100micrometerx100micrometer size, even if it doubles a 8-bit latch of drawing 4 , if 0.25-micrometer submicron technique is used. In a 28 inches SXGA type (1280x1024 pixels) color large-sized display device, as for this size, decreasing 16% can only bear a numerical aperture enough at practical use. Furthermore, if the submicron technical process of 0.15 is used, the decrement in a numerical aperture will become about 5%, and will hardly pose a problem.

[0033] The whole picture image equipment configuration is shown in drawing 9 . The glass plates 102 and 103 of two sheets are made to counter through the micrometers [ several ] space 105, and it fixes, and has the structure which enclosed liquid crystal 100 between them. The image display circuit 104 where all the image display element circuits that contain the data bus prepared in train correspondence and a latch of each pixel correspondence, and a DA converter by this invention other than a common electrode and a light filter were formed on the up glass substrate 102 is arranged. These are inserted with two polarizing plates 101, and if incidence of the white light is carried out, it will become penetrated type display from the lower part of drawing 9 .

[0034] Furthermore, the control circuit, X drive circuit, and Y drive circuit which are shown in the display of drawing 9 in drawing 1 can also be made, and it is the so-called system. Inn It can also consider as a display.

[0035] In addition, with the gestalt of this operation, although the current change type DA converter was used, even if it constitutes from a resistance assembled die which replaces with this and consists of resistance, or a capacitive component split mold, the same effect is acquired.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] The circuit-arrangement view showing the gestalt of 1 implementation of the image display equipment by this invention.
[Drawing 2] The timing chart showing the signal change for explaining an operation of drawing 1 .
[Drawing 3] The notation display circuit block diagram (a) and gate display circuit block diagram (b) of a latch of drawing 1 .
[Drawing 4] The notation display circuit block diagram (a) and gate display circuit block diagram (b) of an inverter of drawing 1 .
[Drawing 5] The notation display circuit block diagram (a) and gate display circuit block diagram (b) of a DA converter of drawing 1 .
[Drawing 6] The notation display circuit block diagram (a) and gate display circuit block diagram (b) of an operational amplifier of drawing 1 .
[Drawing 7] The gate display circuit block diagram of the bias voltage occurrence circuit for the operational amplifiers of drawing 1 .
[Drawing 8] The cross section showing the circuit formation section of the image display equipment of drawing 1 .
[Drawing 9] The decomposition perspective diagram showing the whole image display equipment configuration of drawing 1 .
[Drawing 10] The circuit-arrangement view of the conventional image display equipment.
[Description of Notations]
14 [ -- A DA converter, 21 / -- Latch, ] -- A display pixel, 23 -- TN liquid crystal layer electrostatic capacity, 22 11 [ -- A data bus, 16 / -- X drive circuit, ] -- A gate line, 15 -- Y drive circuit, 12 19 [ -- A common electrode, 17 / -- Clock, ] -- A control circuit, 20 -- A signal input terminal, 24 18 [ -- The output current line of positive/negative, ] -- A digital input line, 41 -- The DA converter of MSB, 42, 43 44 [ -- Polycrystal silicon layer, ] -- A current-voltage converter, 45 -- An operational amplifier, 80 81 [ -- Drain electrode, ] -- An insulating substrate, 83 -- A channel formation field, 84 85 [ -- A gate electrode, 88 / -- Drain diffusion layer, ] -- A source electrode, 86 -- A gate insulator layer, 87 89 [ -- p type channel TFT, 100 / -- An image display element, 101 / -- A polarizing plate, 102 / -- A lower glass substrate, 103 / -- An up glass substrate, 104 / -- A light filter, 105 / -- Liquid crystal ] -- A source diffusion layer, 90 -- N type channel TFT, 91

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DRAWINGS

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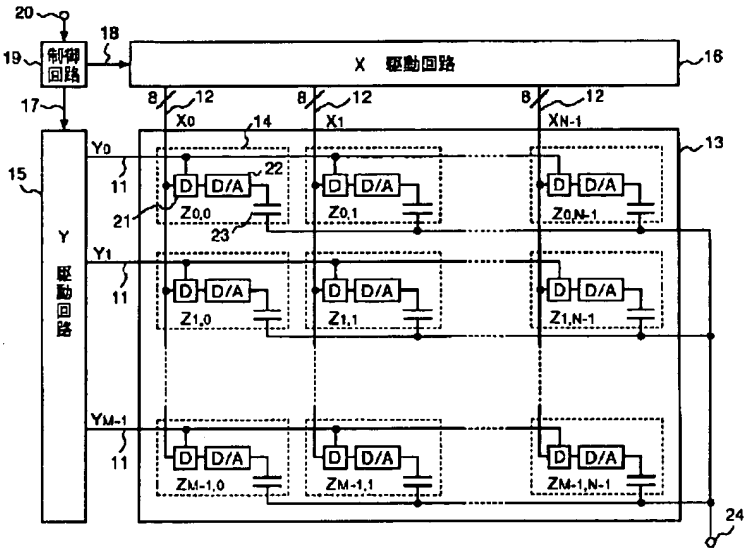
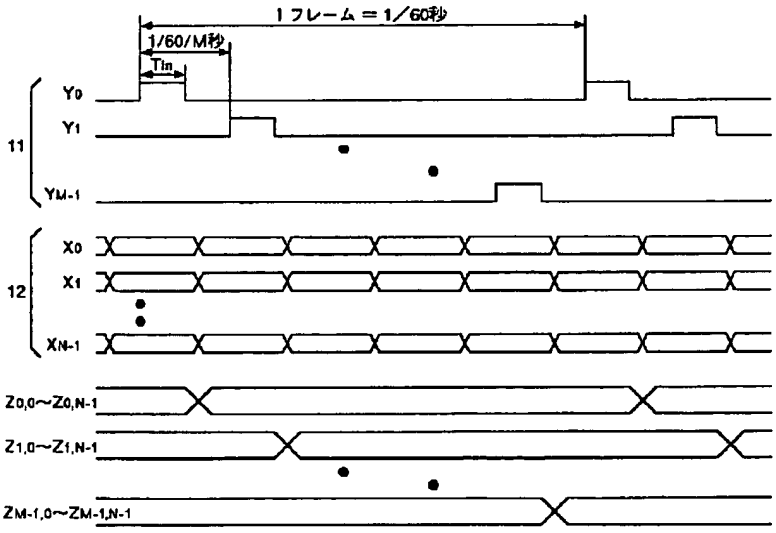
[Drawing 1]

図 1



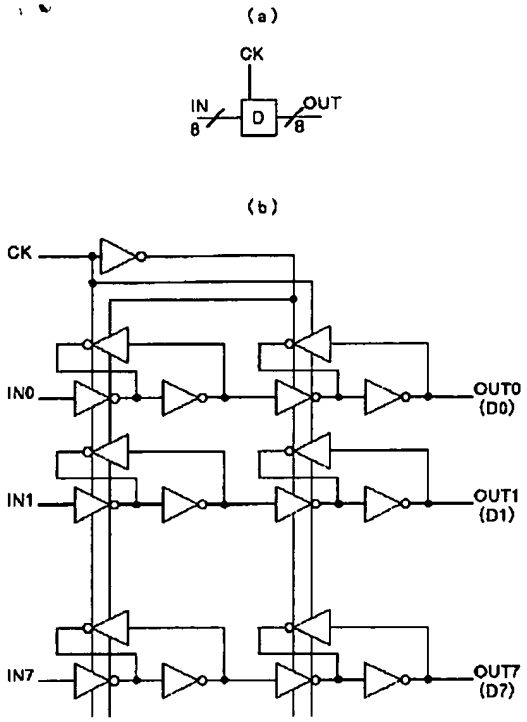

[Drawing 2]

図 2



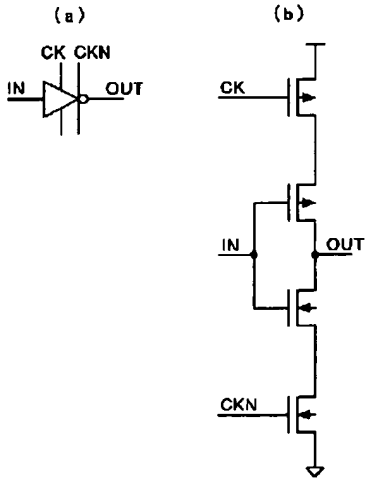

[Drawing 3]

図 3



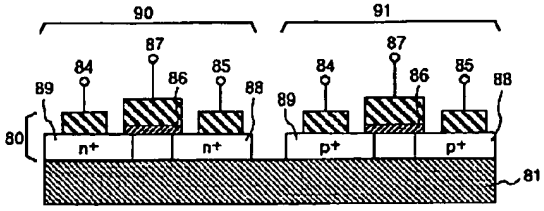

[Drawing 4]

図 4



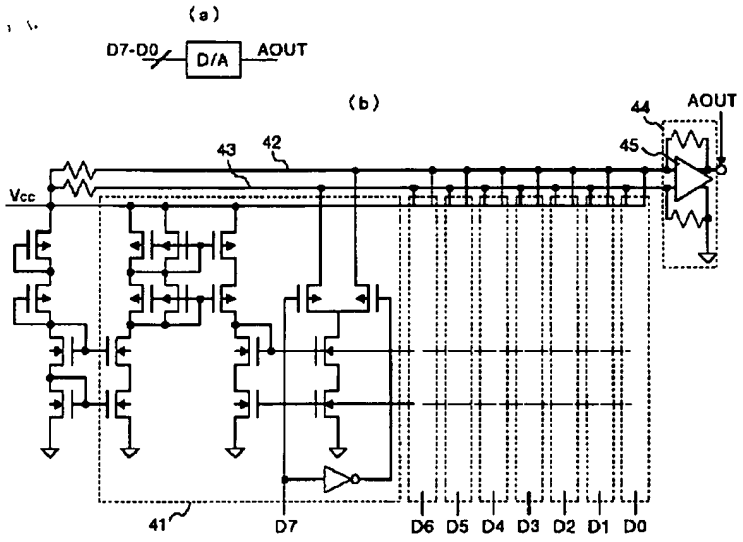

[Drawing 8]

図 8



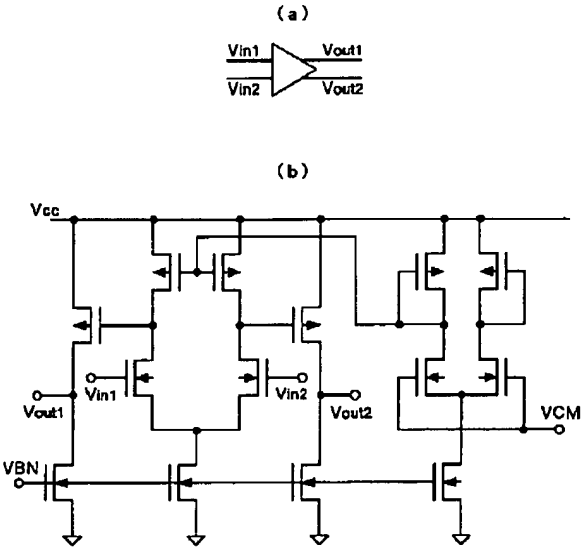

[Drawing 5]

図 5



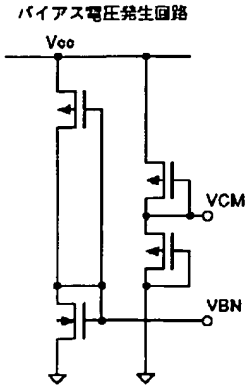

[Drawing 6]

図 6



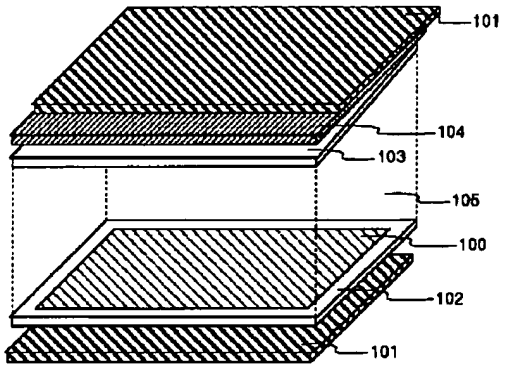

[Drawing 7]

図 7



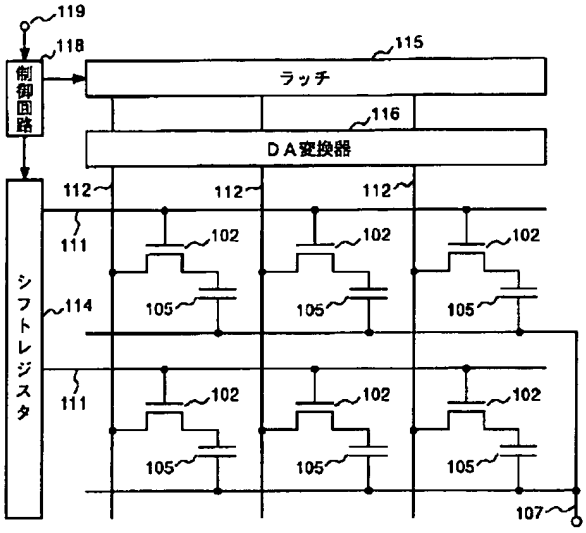
[Drawing 9]

図 9




[Drawing 10]

図 10

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[Translation done.]